

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1 1. An automatic timing analyzer of testing electronic circuits comprising:
2 a first timer for performing a coarse timing measurement of an
3 electronic circuit;
4 a second timer for performing a fine timing measurement of the
5 electronic circuit; and
6 storage means for storing timing measurements of the first and second
7 timers.
- 1 2. The automatic timing analyzer recited in claim 1, wherein the electronic
2 circuits are integrated circuits and the timing analyzer is a component of a
3 Built In Self Test (BIST) system on an integrated circuit.
- 1 3. The automatic timing analyzer recited in claim 2, wherein the BIST system
2 includes separately controlled delay elements for controlling timing of output
3 signals for said first and second timers.
- 1 4. The automatic timing analyzer recited in claim 3, wherein the delay
2 elements are controlled by individual control words.
- 1 5. The automatic timing analyzer recited in claim 4, wherein the control words
2 are generated from a bank of binary counters.
- 1 6. The automatic timing analyzer recited in claim 5, wherein relative timing of
2 output signals is adjusted by incrementing or decrementing respective

3 counters in the bank of binary counters.

1 7. The automatic timing analyzer recited in claim 5, wherein a set of control
2 words are stepped through by the bank of binary counters.

1 8. An integrated circuit having a Built In Self Test (BIST) system which
2 includes a first timer for performing a coarse timing measurement of the
3 integrated circuit, a second timer for performing a fine timing measurement of
4 the integrated circuit, and storage means for storing timing measurements of
5 the first and second timers.

1 9. The integrated circuit recited in claim 8, wherein the BIST system is used to
2 test effects of timing skews between multiple stimuli.

1 10. The integrated circuit recited in claim 9, wherein all possible combinations
2 of a plurality of timing signals and a plurality of timing variations are tested.

1 11. A method of testing electronic circuits comprising the steps of:
2 performing a coarse timing measurement of an electronic circuit;
3 performing a fine timing measurement of the electronic circuit; and
4 storing the coarse and fine timing measurements.

1 12. The method of testing recited in claim 11, further comprising the step of
2 controlling timing signals for said coarse and fine timing measurements.

1 13. The method of testing recited in claim 12, wherein the step of controlling
2 is performed using individual control words.

1 14. The method of testing recited in claim 13, further comprising the step of
2 generating the individual control words with a bank of binary counters.

1 15. The method of testing recited in claim 14, further comprising the step of
2 incrementing or decrementing respective counters in the bank of binary
3 counters to adjust relative timing for said coarse and fine testing
4 measurements.